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A SELF-COMPENSATING ELECTRONIC INTEGRATOR FOR THE PROTON LABORATORY

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FIGURES

INTRODUCTION

Figure 1 is an electric diagram of a simple current integrator presently used in the Proton Laboratory to measure loss monitor and SEM outputs.

The integrator is a high gain amplifier (K = 50,000) with an integrating capacitor connected from the output of the amplifier back to its inverting input. A description of the integrator assumes that the input port of the amp draws no current and that the input resistance to the amp is infinite, i.e.,

Input current $I_{IN} = 0$ 1

Input resistance $R_{IN} = \infty$ 2

Any current applied to the input port will charge up the integrating capacitor hence the output must rise such that:

$$Q = -CE \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad . \quad 3$$

where: Q = charge in coulombs

C = size of the capacitor in Farads

E = volts

but: $I = \frac{dQ}{dt}$ (current)

$$\int Idt = Q$$

$$\int Idt = -CE$$

$$\int Idt = E$$

(the negative sign comes from the fact that the amplifier is connected in an inverting mode). Unfortunately, in the real world, the input port of the amp does draw some current known as the offset current. Hence, the real output of an integrator is:

$$E_{OUT} = -\frac{1}{C}\int I_{IN}dt + \int I_{OFFSET}dt \quad \ldots\ldots\ldots\ldots 5$$

So, here we have the trouble with integrators, that is, for no input, the output will rise to a value of:

$$-\frac{1}{C}\int I_{OFFSET}dt \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 6$$

You may tend to say, "So what?", let's just measure this offset current and subtract it from the final output. The fault in doing so is that the offset current is a function of many things, e.g.,

1. Temperature.
2. Humidity.
3. External currents loops or paths caused by dirt or moisture.
4. Long term aging of a device.
5. Offsets introduced from the device being monitored which are subject to its own list of variables, i.e., SEMs and loss monitors.

This paper then describes an integrator designed, built, and currently running in the Proton Lab which monitors all of the "lumped" offsets and algebraically subtracts them from the output every machine cycle. That is, if the offset took a departure from the norm of say ± 400 counts, the output measurement would not change! I think it is fair to say that existing integrators do offer a way to null out offsets; however, they cannot null out a change in offset. That is, if a change in offset of ± 400 counts did occur, the present integrator would pass this change to its output.

OPERATION

The input may be from a SEM or loss monitor. The gating is a switch which will pass any part or all of a signal to the integrator. For the purpose of a circuit description, let us assume the following:

Machine cycle = 12 seconds

Energy = 400 GeV

Flattop = Spill = t_5 to t_5 + 2 seconds

Integration Time = Spill = t_5 to t_5 + 2 seconds

This descritpion refers to Figure 2. During a time interval equal to but not during the spill the integrator is gated on and the offset is allowed to accumulate. This time may be

t_1 to t_1 + 2 seconds

at the end of t_1 + 2 seconds the accumulated offset is placed in memory, inverted by the inverter and applied to the Summing Amplifier. The Summing Amplifier is a device with a mathematical function of:

$$E_{OUT} = E_{IN_1} + E_{IN_2} + E_{IN_3} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots 7$$

Now during t_5 to t_5 + 2 seconds, the integrator is allowed to accumulate charge equal to the $\int$input + $\int$offset and is also applied to the Summing Amplifier. So, therefore, at the end of t_5 + 2 seconds, the Summing Amplifier would output:

$$E_{OUT} = -\frac{1}{C}\int I_{IN}dt - \frac{1}{C}\int I_{OFFSET}dt + \frac{1}{C}\int I_{OFFSET}dt + REF \rightarrow$$

$$= -\frac{1}{C}\int I_{IN}dt + REF \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots 8$$

which is identical to equation 4. That is, output with no offset added, "THE THEORETICALLY PERFECT INTEGRATOR". The obvious advantage of this system is that if the offset takes a departure from the norm, the electronics will automatically cancel it out. Keep in mind that both positive and negative departures will be nulled out. The reference voltage does several things. First, it allows the output to be set to some non-

zero value because zeros may mean that the electronics are not working. Second, the Camac electronics is such that it will handle only positive numbers so this reference sets the output to some positive number so any change in the output may be observed. Third, the setting of the reference can be used to null out all lumped errors in the electronics that may cause the output to be excessively away from zero.

The obvious advantages of this integrator are:

1. Long term stability.
2. No need for adjustment.
3. Guarranteed offset counts.

In addition to the obvious advantages, there are several advantages that are not so obvious:

1. The set output, i.e., the reference voltage, is outputted during the interval t_1 to t_1 + 2 seconds and could be sampled by an experimenter.
2. The real offset is outputted during the interval (plus the reference) t_1 + 2 seconds to t_5 and could be sampled by an experimenter.
3. The integrator can be interchanged with other devices without regard to its intrinsic offset. That is, if 2 Sems have different offsets associated with them, the integrator will automatically compensate.

The proposed integrator gets the timing from the existing 091 module presently used to run the standard integrators (See Figure 3). In this way the integrate and compensation windows can be changed through the MAC computer. If desired a design change can be incorporated to allow the compensation window to be internal and will automatically adjust to be identical to the integrate window. In the discussion of sampling

times, t_1 was chosen as the compensating time. In practice the reference times would be T_5 because then one could use the same 091 card for both integration and compensation.

TESTING

Figure 4 is a photograph of the output with beam off with an offset of 160 counts inputted to the device. During this time t_1 to t_1 plus 2 seconds the device showed 10 counts output. This was the value of the reference voltage (1 millivolt = 1 count). From the time t_1 plus 2 seconds to t_5 the device showed the accumulated offset plus the reference. During the spill, you can see the offset reducing towards zero. The time after spill (t_6) shows the value that was outputted. It is interesting to note at this time that the stored value of offset is not subject to droop since the memory is an analog to digital converter. Therefore, one need not be concerned when the compensation sample is done.

The integrator was connected to SE615 and allowed to run. The standard integrator was then used and allowed to run. Both times the outputs were compared to SE616. Figure 5 is a graph of the tracking of the new integrator to the standard integrator with beam on.

Figure 6 is a histogram of the actual output counts when the reference was set to 10_{MV}. The plot has been normalized to zero. Looking at the graph one can see that the full width is 10. That is, the output will deviate $\pm$ 5 counts around the set point for the reference voltage.

Figure 7 is a graph of what you can expect as an output as the real offset varies. It is the graph that is the most impressive since you can see that the output really does not change with offset. In fact the output variation is no longer a function of the offset.

CONCLUSION AND RECOMMENDATION

The proposed integrator offers several advantages over the existing ones. The most impressive is the fact that the output count does not change with a change in offset. However, the spread of the output (approximately 5 mv) may seem a bit excessive. But remember this output would not change outside of this number.

Several things could be incorporated at a second look at this design. They are:

1. Remote gain.
2. Internal timing.
3. Reducing the spread in output.

The remote gain could simply be a relay closure to switch in a different integrating capacitor.

The internal timing that I mentioned above means that the integrator could be made "smart enough" to set its own compensating window to be equal to the integration window. The closer this compensating window is to the integration window (in length) the better the result will be. In fact, this difference in window lengths may be the reason for the spread in the output counts. Also several of the chips could be eliminated if one were very clever, i.e., the tie between the A/D and D/A could be arranged such that inversion would be automatic and the inverter operational amplifier could be eliminated, etc. However, these things are frills. The present performance is such that it can be placed in service at once.

DATA FOR FIGURE 5

Ratio		Difference
1.02	3680/3575	105
1.01	3957/3880	77
1.03	3510/3397	113
1.0	4340/4307	33
1.04	3432/3290	142
1.01	4012/3975	37
1.01	4052/4000	52
1.03	4040/3920	120
1.01	4545/4510	35
1.08	4117/3785	18
1.01	3845/3827	18
1.00	3347/3345	2
1.01	3505/3442	63
1.01	3832/3807	25
1.02	3680/3600	80
1.01	3612/3570	42
1.02	4057/3975	82
1.05	3435/3272	163
1.04	3805/3642	163
1.02	3600/3530	70
1.03	3242/3130	112
1.04	3922/3772	150
1.04	3500/3342	158
1.03	3340/3240	100
1.04	2952/2825	127
1.02	2812/2747	65

Ratio		Difference
1.04	2332/2235	97
1.04	3357/3207	150
1.04	2987/2857	130
1.04	2425/2325	100
1.04	2120/2032	88
1.04	2242/2150	92
1.	1710/1700	10
1.02	2912/2842	70
1.04	3015/2880	135
1.04	3010/2875	135
1.02	2712/2652 2812/2747	60
1.02	955/932	23
1.04	3017/2885	132
	40/110	70

A STANDARD INTEGRATOR

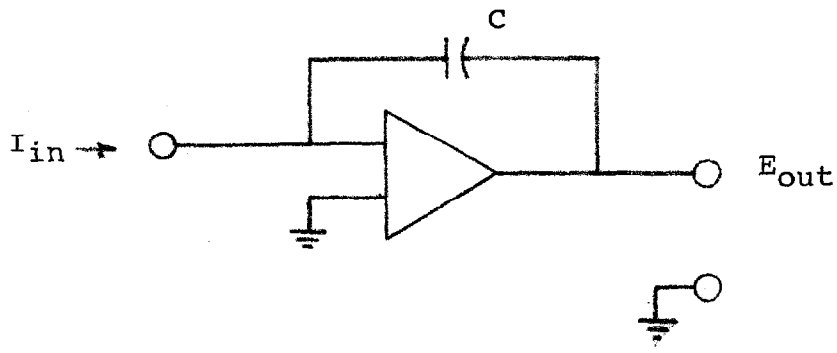


FIGURE 1

A BLOCK DIAGRAM OF THE NEW STYLE INTEGRATOR

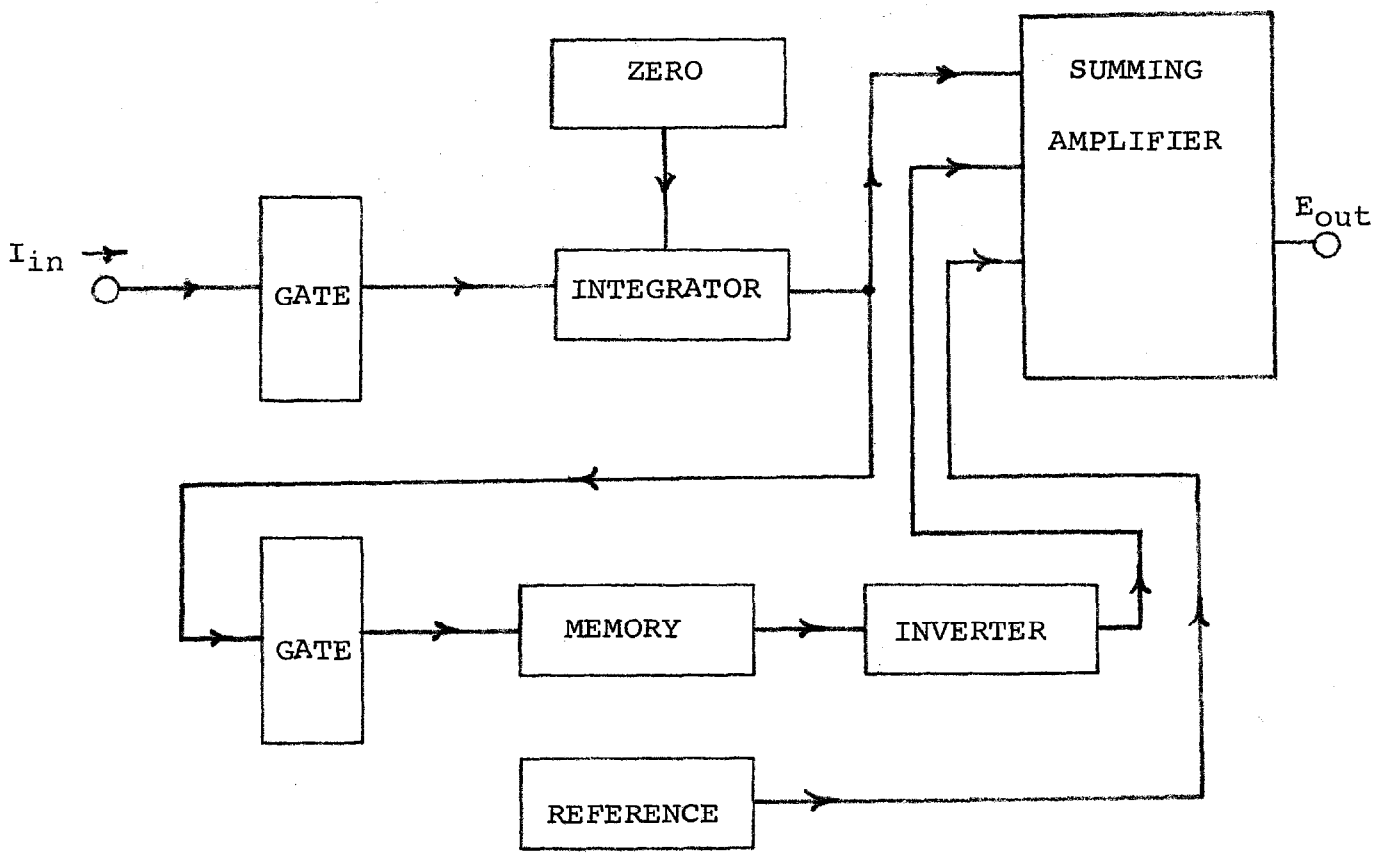


FIGURE 2

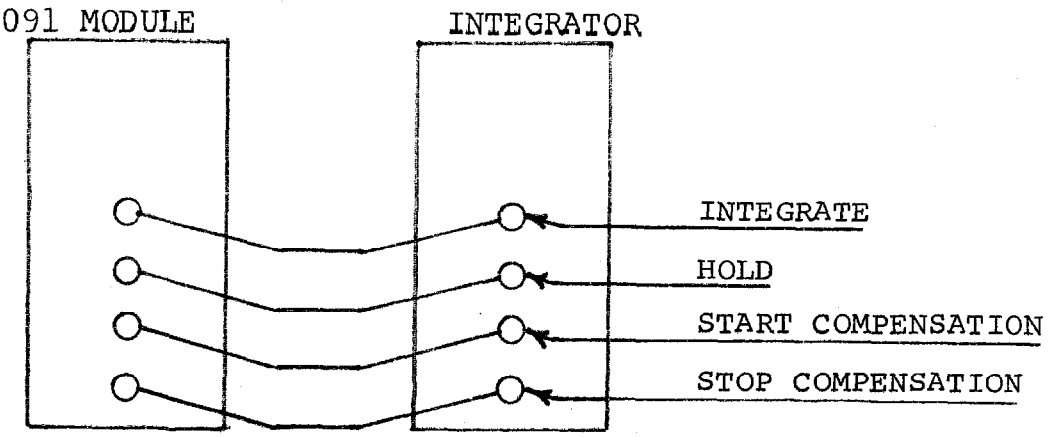
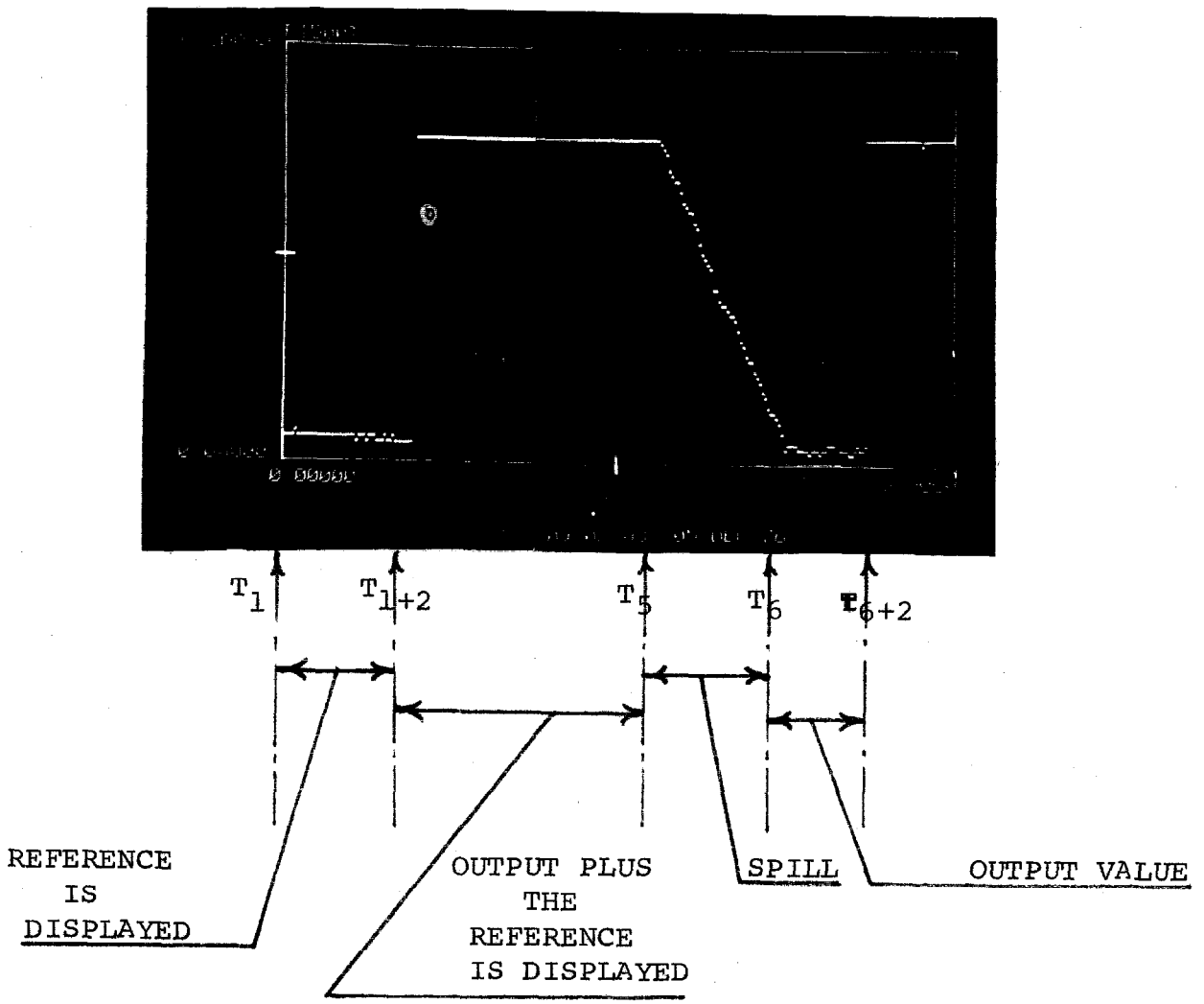


FIGURE 3



A photograph of the integrator output with beam off.

FIGURE 4

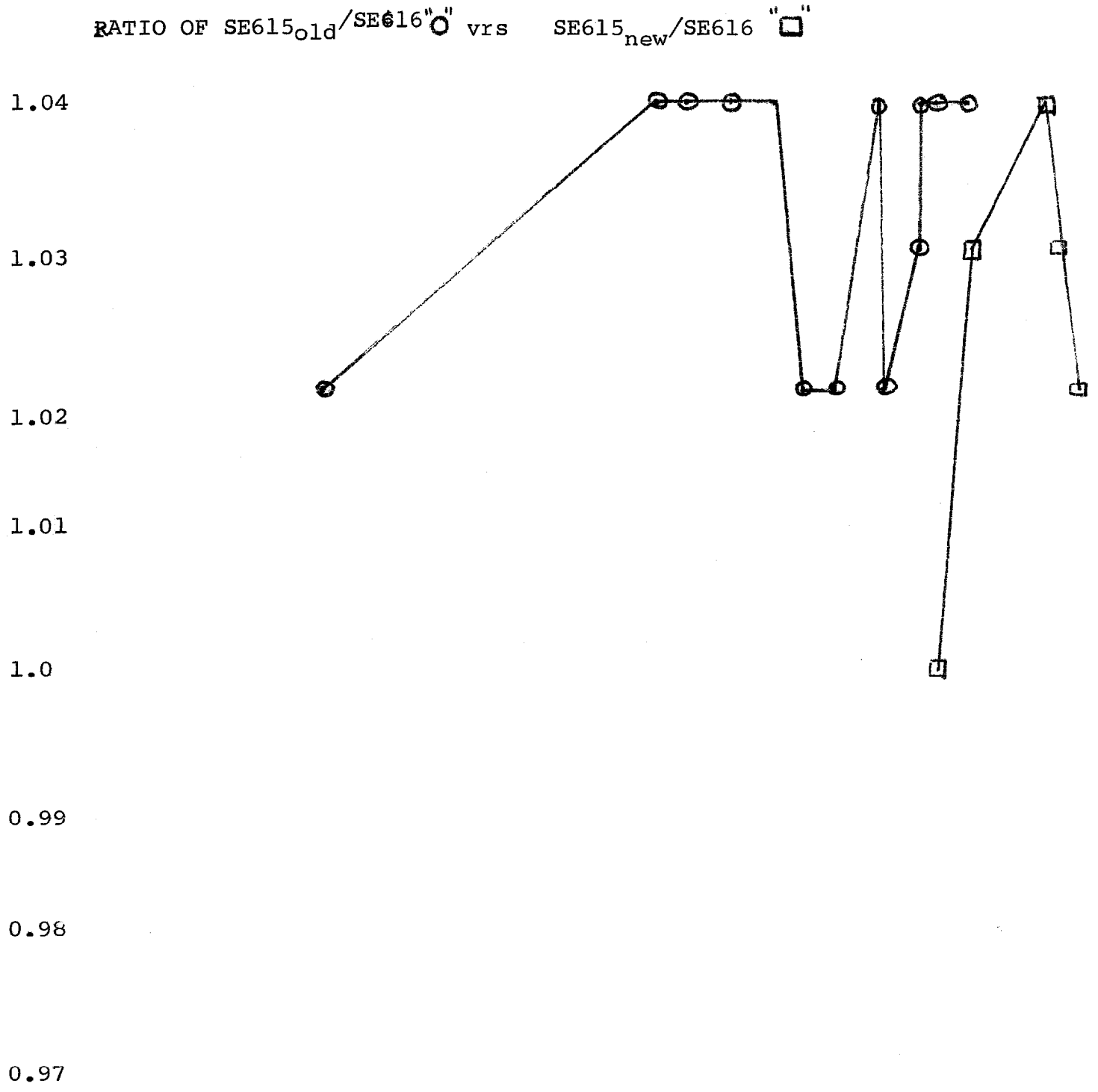
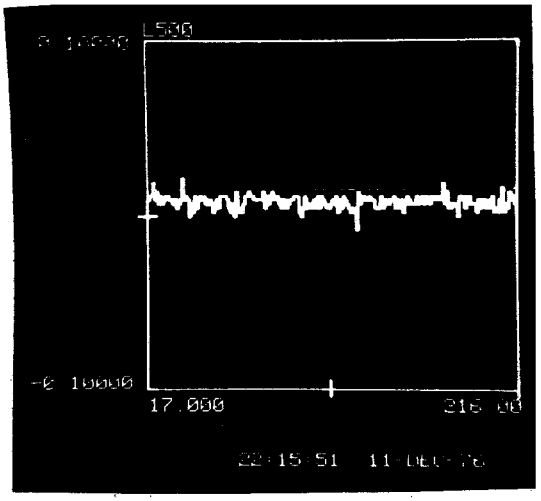

RATIO OF SE615old/SE616"O" vrs SE615new/SE616 "□"
1.04
1.03
1.02
1.01
1.0
0.99
0.98
0.97
These ratios are with beam one
0
500
1000
1500
2000
2500
3000
3500
RATIO
INTENSITY

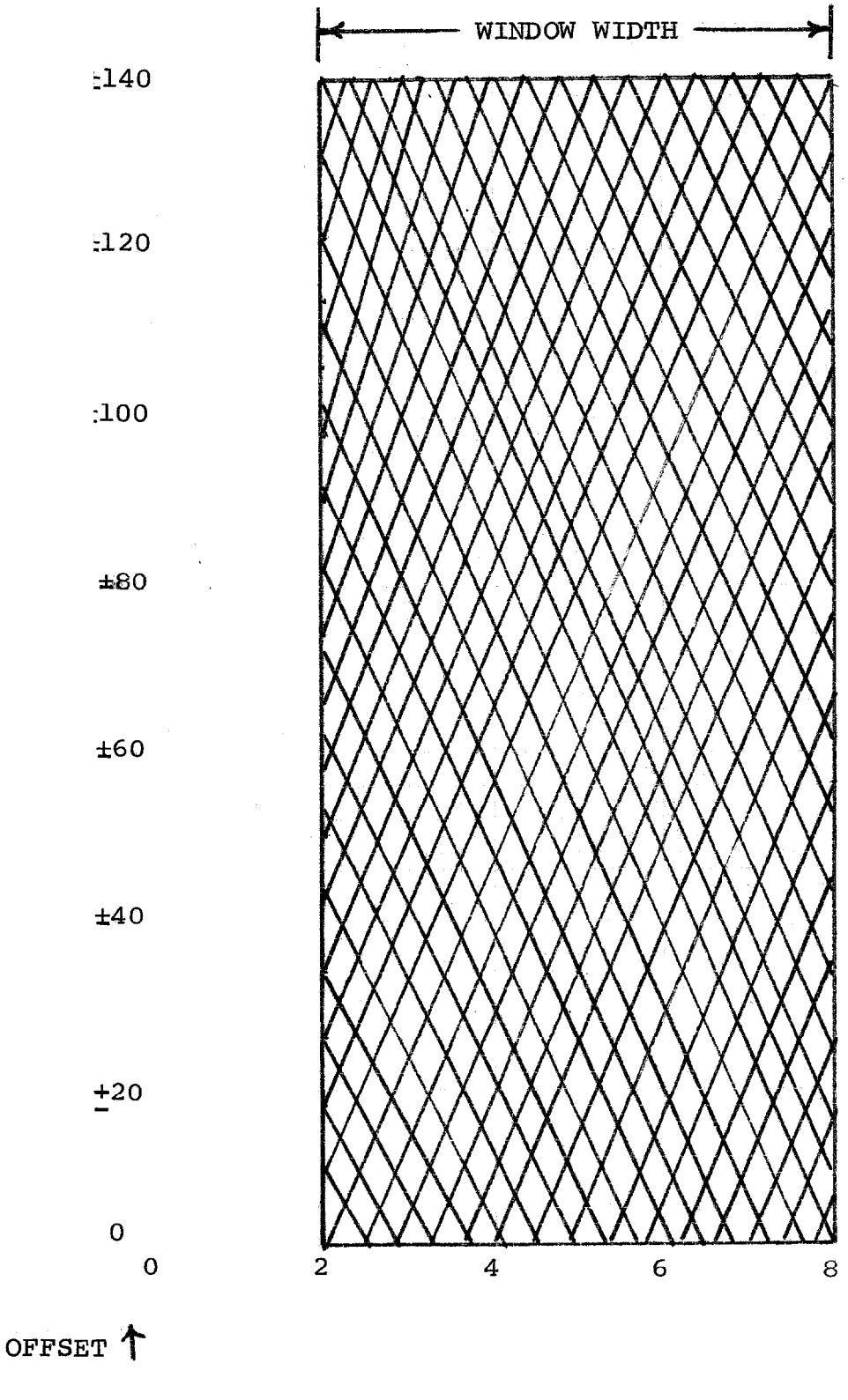
FIGURE 5



A PHOTOGRAPH OF THE INTEGRATORS OUTPUT OVER A PERIOD OF ONE HOUR. THE OUT PUT IS AROUND 10 MILIVOLTS. THIS RECORD IS WITH BEAM OFF AND WITH ALL CABELING CONNECTED.

FIGURE 6

OUTPUT COUNTS VRS. LARGE DEVIATIONS IN INPUT OFFSET



THE CROSSHATCHED AREA OF THIS GRAPH SHOWS THAT FOR LARGE DEVIATIONS IN OFFSET VALUES THE OUTPUT WILL REMAIN IN ITS GUARANTEED WINDOW OF SIX COUNTS.

FIGURE 7

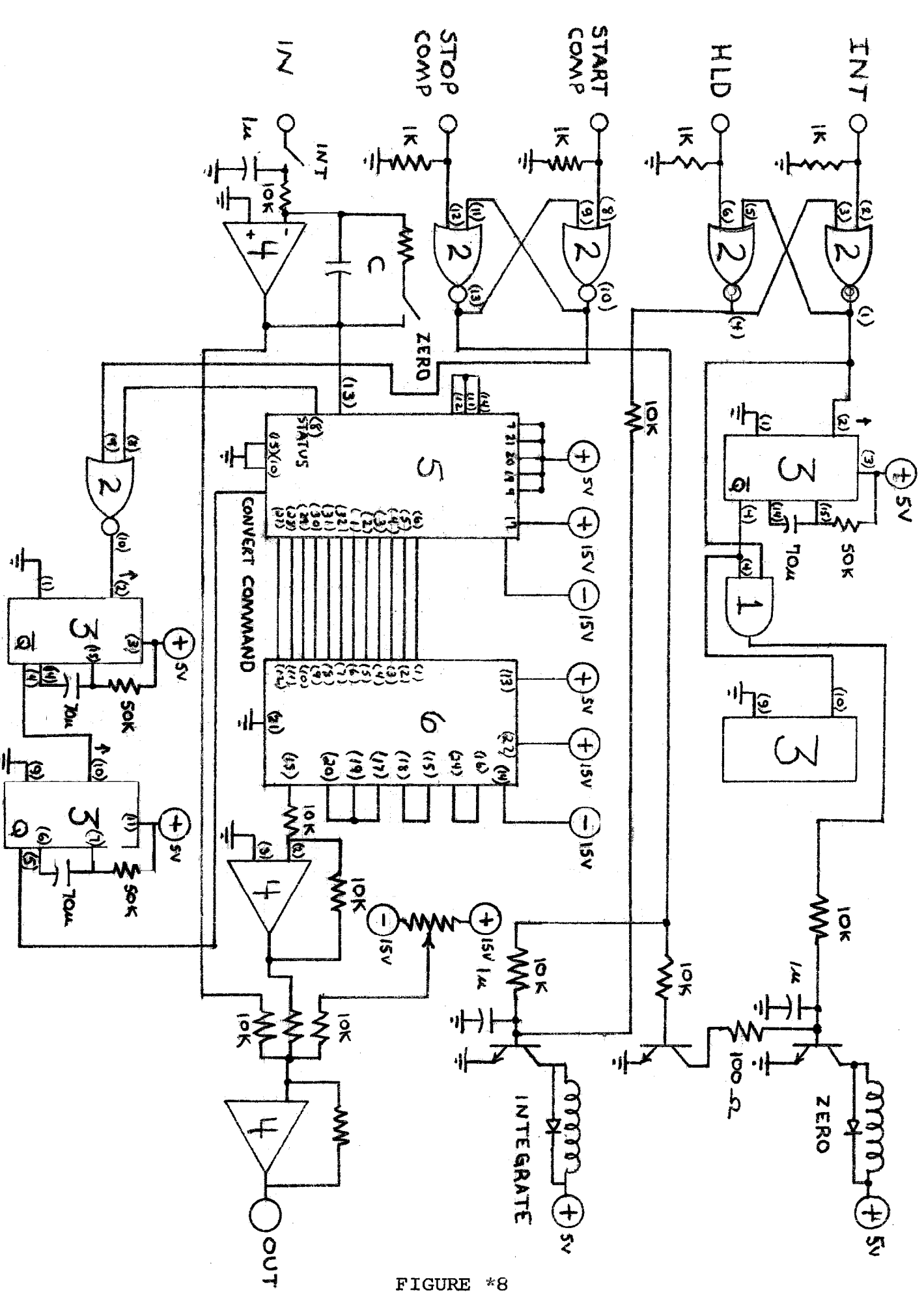

IN
STOP COMP
START COMP
HLD
INT
1K
10K
1μ
INT
ZERO
C
CONVERT COMMAND
STATUS
5V
15V
-15V
50K
70K
10K
100Ω
INTEGRATE
OUT

FIGURE *8